REMARKS

Claims 1-13 and 20 are pending in this application.

Previous claims 1-8 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Warren et al. (US Patent 6,075,807) in view of Tweed et al (US Patent 5,818,769). Previous Claims 9-13, 19-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Warren et al. (US Patent 6,075,807) in view of Alexander (US Patent 6, 765, 419 B2). Previous claims 15-17 have been rejected under 35 USC 102(b) as anticipated by Tweed. Previous Claim 18 has been rejected under 35 USC 103(a) as unpatentable over Tweed in view of Warren.

Claims 14-19 have been cancelled without prejudice, to further expedite prosecution of remaining claims. Having regard to the Examiner's comments and for better defining the invention, claims 1, 8, 9 and 13 have been amended.

Without limitation of the claims, the disclosed embodiments pertain to digital processing of data samples and to data path latency due to processing of samples through delay chains. Delay chains are introduced within digital systems to allow for various transient processing operations, such as timing recovery of samples' boundaries in the case of data packets. However, the processing of samples through such delay chains subsequent to the transient processing events that required them may unnecessarily add to the data path latency and, consequently, lead to suboptimal performance. Disclosed embodiments provide for reduction of the data path latency via reduction of the length of such delay chains once the transient processing operations are completed. In particular, dynamic reduction of the length of a delay chain no longer required is provided by eliminating delay elements from the delay chain, which is achieved by shifting samples out of the delay chain at an output rate higher than an input rate of reading additional samples into the delay chain. In the preferred embodiments, the shifting of elements through selected sections of the delay chain, at selected clock cycles, is facilitated by enable signals associated with each data storing element in the chain.

Rejection of Claims 1-8 under 35 U.S.C. 103(a) as unpatentable over Warren et al. in view of Tweed et al

The Examiner has rejected previous claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over Warren in view of Tweed.

With respect to previous claim 1, on page 4 of the Office Action, the Examiner indicates that *Warren discloses a method of reducing data path latency in digitally processing a sequence of data samples.* Nonetheless, the Examiner also indicates on page 2 of the Office Action, in the Response to Remarks section, first paragraph, that he agrees with the Applicant' s assertion from the previous communication that "Warren does not disclose nor otherwise suggest reducing the length of a delay line". Therefore, the Examiner's assertion that Warren discloses a method of reducing data path latency in digitally processing a sequence of data samples is believed to be in error.

For further clarity, Applicant reaffirms that Warren does not disclose nor otherwise suggest a method of reducing data path latency. Applicant indicates that Warren is directed at a receiver adapted to despread digital signals using two or more different code lengths and rates. The Warren receiver in Figure 1 has an associated tapped delay line, 12, having K stages, 14_1 to 14_K. Of the K stages, all of them are sampled by a first correlator 20 corresponding to a spreading code of length M, where M is less than or equal to K, but only N of the stages are sampled by a second correlator 30 corresponding to a spreading code of length N, where N is less than K. Therefore, Warren discloses all data values of a delay line being sampled by correlator 20, while only a subset being sampled by correlator 30 at the same time. However, there is no disclosure in Warren of the tapped delay line 12 as being reduced in length. For each of the two correlators using its data, the delay line 12 has the same length, at all times, i.e. length K for correlator 20 and length N for correlator 30. Sampling only a subset of the values of the line is not equivalent to reducing the data path latency, as claimed in claim 1.

Further, Applicant contends that Warren does not disclose nor otherwise suggest a method of reducing data path latency, the data path being associated with a transient processing operation on the data samples. In Warren, there is no disclosure of the delay line 12 being reduced in length after a transient operation.

Further with respect to claim 1, the Examiner has relied on Tweed for teaching shifting data samples out of the delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain. To better distinguish over Tweed, claim 1 has been amended to better describe the elements of the delay line as updating their values based on enable signals associated with each element of the line, as well as the shifting of data through the delay line based on selected clock cycles, as follows:

Claim 1: A method of reducing data path latency in digitally processing a sequence of data samples, the data path latency being associated with a transient processing operation on the data samples, comprising:

at the transition into the transient processing operation on the data samples reading the sequence of data samples into a tapped clocked delay chain, wherein each data storing element of the chain has an associated enable signal for controlling, on any given clock cycle, whether to update or not its respective stored data sample;

during the transient processing operation on the data samples, processing data samples from taps on the clocked delay chain;

in response to receiving a signal of completion of the transient processing operation on the data samples, controlling the enabling signal of each data storing element in the chain to allow shifting data samples through an end portion of the clocked delay chain on a selected first set of clock cycles determining a first shifting rate and shifting data samples in an initial portion of the delay chain on a selected second set of clock cycles determining a second shifting rate, wherein the initial portion is complementary to the end portion and wherein the first shifting rate is higher than the second shifting rate; and

dynamically reducing the length of the clocked delay chain by moving the output of the delay chain to the last data storing element of the initial portion, after a number of clock cycles.

Support for the above claim 1 amendments can be found in the description on pages 5 to 10 and Figures 2 to 6.

Applicant contends that Tweed does not disclose nor otherwise suggest : "*a tapped clocked delay chain, wherein each data storing element of the chain has an associated enable signal for controlling, on any given clock cycle, whether to update or not its respective stored data sample*", nor "*controlling the enabling signal of each data storing element in the chain to allow shifting data samples through an end portion of the clocked delay chain on a selected first set of clock cycles determining a first shifting rate and shifting data samples in the complementary initial portion of the delay chain on a selected second set of clock cycles determining a second shifting rate, wherein the first shifting rate is higher than the second*

shifting rate", nor "*dynamically reducing the length of the clocked delay chain by moving the output of the delay chain to the last data storing element of the complementary end portion, after a predetermined number of clock cycles".*

Applicant further contends that none of these limitations are disclosed by any of the remaining cited art references.

Based on at least this reasoning, the Applicant believes that Claim 1 is patentable over the cited art. The Applicant further contends that independent Applicant contends amended method claim 8 and amended apparatus claims 9 and 13 reciting limitations of claim 1, in the same or similar language, are also patentably distinct over the cited art for reasons presented in regards to claim 1.

As claims 2-7 are dependent directly or indirectly on claim 1 and incorporate its limitations, claim 10-12 are dependent directly or indirectly on claim 9 and incorporate its limitations and claim 20 is dependent on claim 13 and incorporates its limitations, the Applicant also respectfully asserts that the cited prior art references, taken alone or in combination, fail to teach, suggest or otherwise render obvious claims 2-7, 10-12 and 20. Therefore, Applicant asserts that claims 2-7, 10-12 and 20 are also allowable over the cited art.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Concord, MA 01742-9133
Date: December 3, 2009